AMENDMENTS TO THE CLAIMS:

Please cancel claims 13-20 and 25-27 without prejudice or disclaimer.

1. (Original) A semiconductor device, comprising:

a strained-silicon channel formed adjacent a source and a drain;

a first gate formed over a first side of said channel;

a second gate formed over a second side of said channel;

a first gate dielectric formed between said first gate and said strained-silicon channel; and

a second gate dielectric formed between said second gate and said strained-silicon channel,

wherein said strained-silicon channel is non-planar.

2. (Original) The device of claim 1, wherein said strained-silicon channel thickness is substantially uniform.

3. (Original) The device of claim 1, wherein said strained-silicon channel thickness is set by epitaxial growth.

4. (Original) The device of claim 1, wherein said strained-silicon channel is substantially defect-free.

5. (Original) The device of claim 1, wherein said strained-silicon channel includes a distorted lattice cell.

6. (Original) The device of claim 1, wherein said first gate and said second gate are independently controllable.

7. (Original) The device of claim 1, wherein said strained-silicon channel comprises a fin.

8. (Original) The device of claim 1, wherein said first gate and said second gate are self-aligned.

9. (Original) The device of claim 1, wherein said first gate and said second gate are defined in a single lithographic step.

10. (Original) The device of claim 1, wherein said first gate, said second gate, said source and said drain are self-aligned with respect to each other.

11. (Original) The device of claim 7, further comprising a plurality of fins.

12. (Original) The device of claim 1, wherein said device includes a planarized top surface.

13. (Canceled)

14. (Canceled)

15. (Canceled)

16. (Canceled)

17. (Canceled)

18. (Canceled)

19. (Canceled)

20. (Canceled)

21. (Original) A semiconductor device, comprising:

a strained-silicon channel formed adjacent a source and a drain;

a first gate formed over a first side of said channel;

a second gate formed over a second side of said channel;

a first gate dielectric formed between said first gate and said strained-silicon channel; and

a second gate dielectric formed between said second gate and said strained-silicon channel,

wherein said strained-silicon channel comprises a fin.

22. (Original) A circuit, comprising:

the semiconductor device of claim 1.

23. (Original) The device of claim 1, wherein said strained-silicon channel is tensely strained.

24. (Original) The device of claim 1, wherein said strained-silicon channel is compressively strained.

25. (Canceled)

26. (Canceled)

27. (Canceled)

28. (New) The device of claim 1, wherein the first gate is electrically separated from the second gate.

29. (New) The device of claim 21, wherein the first gate is electrically separated from the second gater.

30. (New) A semiconductor device, comprising:

a strained-silicon channel formed adjacent a source and a drain;

a first gate formed over a first sidewall of said channel;

a second gate formed over a second sidewall of said channel;

a first gate dielectric formed between said first gate and said strained-silicon channel; and

a second gate dielectric formed between said second gate and said strained-silicon channel,

wherein said strained-silicon channel is non-planar, and said first and second sidewalls are opposing to each other.

31. (New) A semiconductor device, comprising:

a strained-silicon channel formed adjacent a source and a drain, wherein strain in said strained-silicon channel was elastically induced by a sacrificial stressor;

a first gate formed over a first side of said channel;

a second gate formed over a second side of said channel;

a first gate dielectric formed between said first gate and said strained-silicon channel; and

a second gate dielectric formed between said second gate and said strained-silicon channel, wherein said strained-silicon channel is non-planar, and is fixed to the substrate by said first and second gates.

32. (New) The device of claim 1, wherein said strained-silicon channel is formed by a sacrificial stressor formed over silicon.

33. (New) The device of claim 21, wherein said said strained-silicon channel is formed by a sacrificial stressor formed over silicon.

a second gate formed over a second sidewall of said channel;

a first gate dielectric formed between said first gate and said strained-silicon channel; and

a second gate dielectric formed between said second gate and said strained-silicon channel,

wherein said strained-silicon channel is non-planar, and said first and second sidewalls are opposing to each other.

31. (New) A semiconductor device, comprising:

a strained-silicon channel formed adjacent a source and a drain, wherein strain in said strained-silicon channel was elastically induced by a sacrificial stressor;

a first gate formed over a first side of said channel;

a second gate formed over a second side of said channel;

a first gate dielectric formed between said first gate and said strained-silicon channel; and

a second gate dielectric formed between said second gate and said strained-silicon channel, wherein said strained-silicon channel is non-planar, and is fixed to the substrate by said first and second gates.

32. (New) The device of claim 1, wherein strain in said strained-silicon channel was elastically induced by a sacrificial stressor.

33. (New) The device of claim 21, wherein strain in said strained-silicon channel was elastically induced by a sacrificial stressor.